WHAT IS CLAIMED IS:

1. A memory pumping circuit comprising a DRAM cell used as the charging capacitor of said pumping circuit for enhancing the capacitance.

2. The memory pumping circuit according to Claim 1 wherein said DRAM cell consists of a MOS transistor and a storage cell.

3. The memory pumping circuit according to Claim 1 wherein said pumping circuit comprises a current source to provide a charge current for the DRAM cell.

4. The memory pumping circuit according to Claim 3 wherein said DRAM cell comprises an output port for providing a pumping voltage source; and the output port electrically connects to said current source for getting said charge current.

5. The memory pumping circuit according to Claim 4 wherein said pumping voltage source is a voltage source of a word line.

6. The memory pumping circuit according to Claim 1 wherein a driving circuit generates a clock signal for driving said DRAM cell.

7. The memory pumping circuit according to Claim 6 wherein said driving circuit is an inverter.

8. The memory pumping circuit according to Claim 6 wherein said driving circuit consists of a PMOS transistor and a NMOS transistor, and generates said clock signal according to a first clock signal and a second clock signal.

9. A memory pumping circuit comprises:

a current source for providing a charge current;

a DRAM cell as a charging capacitor of the pumping circuit, said DRAM cell having an output port for providing a pumping voltage source, said output port connecting to said current source for receiving

the charge current; and

a driving circuit for generating a first clock signal to said DRAM cell for driving said DRAM cell.

10. The memory pumping circuit according to Claim 9 wherein said DRAM cell consists of a MOS transistor and a storage cell.

11. The memory pumping circuit according to Claim 9 wherein said pumping voltage source is a voltage source of a word line.

12. The memory pumping circuit according to Claim 9 wherein said driving circuit is an inverter.

13. The memory pumping circuit according to Claim 9 wherein said driving circuit consists of a PMOS transistor and a NMOS transistor, and generates said first clock signal according to a second clock signal and a third clock signal.